

Technical Case Study:

Desktop PCI Packet Processing Engine based on an Intel 2400 Network Processor

This case study highlights a customer who needed help designing a complex and densely populated printed circuit board in a short time frame and demonstrates the importance of process, flexibility, and experience. Stilwell Baker successfully accomplished the customer's goals by recognizing the challenges early, applying our expert technical knowledge, and using multiple designers to meet our customer's needs.

The Problem

The customer's in-house design team faced a technically challenging PCB layout project with a very aggressive delivery schedule. The project involved the layout of a desktop PCI Packet Processing Engine design, which was based on an Intel 2400 Network Processor.

The Intel 2400 processor requires high speed routing to the supporting components and the memory. The high pin density of the processor requires the fan-out and priority of signals to be considered early in the design to avoid adding extra layers and to reduce EMI.



The challenges faced when routing a PCI card of this nature requires that extra care be put into the early stage of the placement and routing to insure enough room is given to route all of the signals and still provide correct return paths and planes for the power and ground.

The aspect ratio and finished thickness of the desktop PCI PCB form factor further increased the PCB design difficulty.

Stilwell Baker's Approach

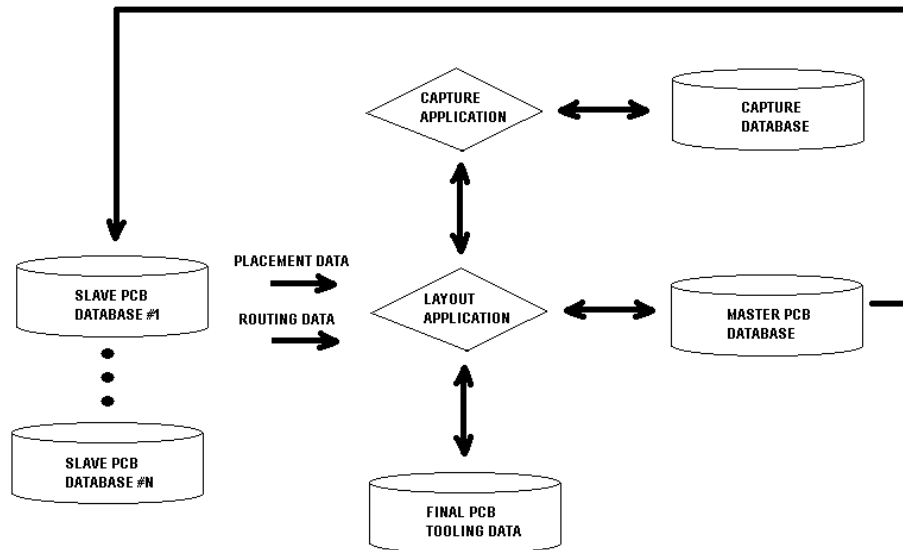
Stilwell Baker provided a senior PCB designer onsite to augment the customer's in-house team. We backed up this lead designer with other resources in Stilwell Baker's Design Center to meet the customer's aggressive schedule. This enabled the lead designer to focus on the technically challenging areas of the design, while additional tasks were performed by offsite resources.

Stilwell Baker's concurrent PCB team design process enabled the design to be routed in parallel and merged during the layout phase. This is explained in detail below.

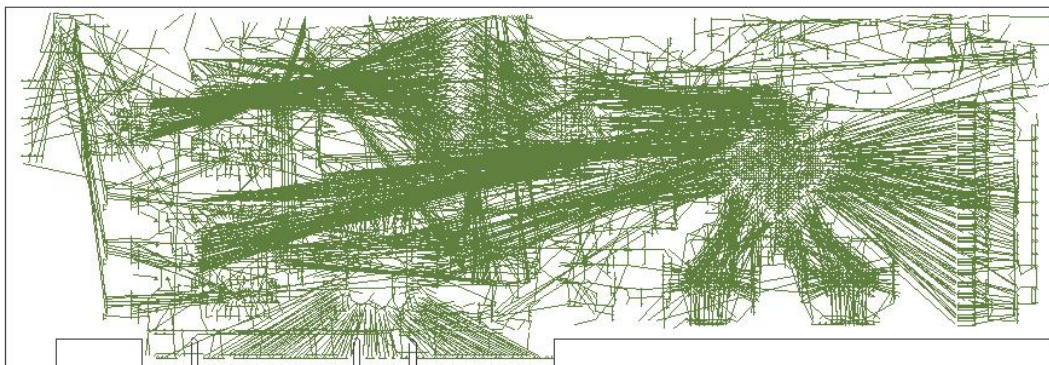
Formalize the PCB routing channel strategy. A formalized PCB routing channel strategy was used to first accurately predict the routing area requirements and to solve this interconnect challenge.

Partition the sub-circuits. We partitioned this PCB's sub-circuits and then distributed them to the available Stilwell Baker and customer resources.

Set up Master and Slave databases. Master and slave PCB databases were merged by Stilwell Baker every 24 hours. Schedule windows were defined within the concurrent PCB layout process for incremental engineering-driven schematic changes.



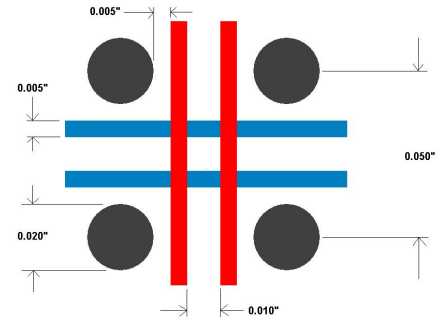
Interconnect the sub-circuits. Serial layout activities were used to interconnect the sub-circuits in the final phases of the PCB layout effort. PCB aspect ratio and maximum finished thickness (~0.065") of the desktop PCI PCB form factor created a horizontal routing bottleneck and limited the number of impedance-controlled signal routing layers available.



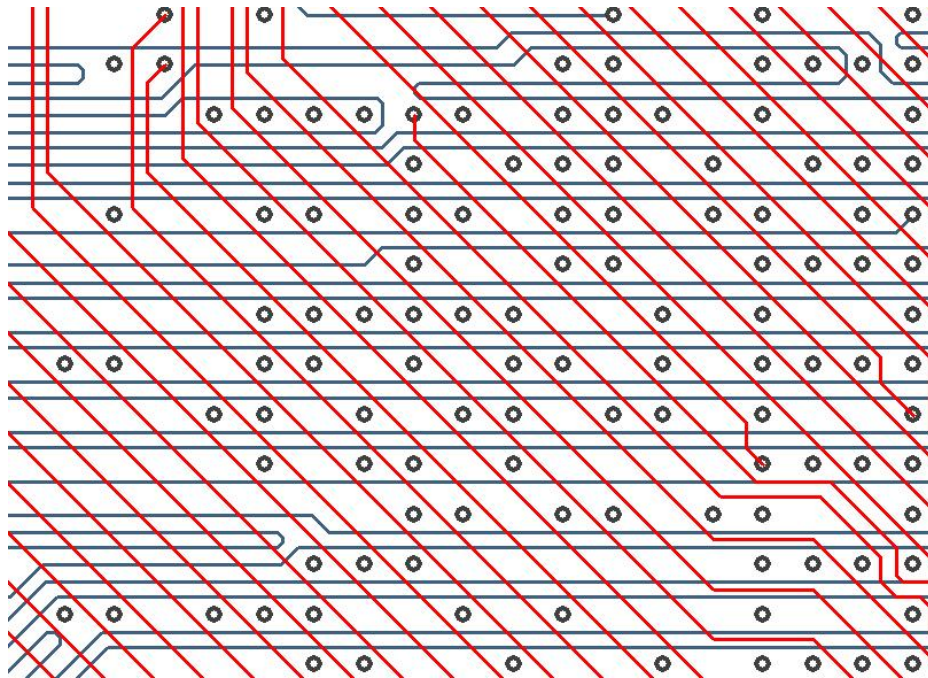
Stilwell Baker's proven PCB channel routing strategy provided an accurate metric for routing area prediction ahead of detailed routing efforts.

Component placement and SMD escape routing respected the formalized coarse via matrix and loosely coupled twin conductor routing channel strategy.

Timing constrained routing specifications were routed using loosely coupled in-channel route meandering.



Use diagonal adjacent diagonal route biasing. Adjacent layer coupling was minimized within the dual stripline routing layer configurations using diagonal adjacent diagonal route biasing.



A Successful Solution

Stilwell Baker helped this customer design a complex and densely populated printed circuit board in a short time frame by bringing to bear our key strengths: a formal process, flexibility, and experience. Stilwell Baker successfully accomplished the customer's goals by recognizing the place & route challenges early, using a proven PCB design process and routing strategy, and using a team of experienced senior designers who worked concurrently to meet the difficult schedule.